What is claimed is:

1. A method for use in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly having a surface; and

forming a barrier layer over the at least a portion of the surface, wherein the barrier layer is formed of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995.

2. The method of claim 1, wherein x is in the range of about 0.90 to about 0.98.

3. The method of claim 2, wherein x is about 0.95.

4. The method of claim 1, wherein forming the barrier layer includes forming the barrier layer by chemical vapor deposition.

5. The method of claim 1, wherein the portion of the surface is a silicon containing surface.

6. A method for use in the formation of a capacitor, the method comprising:

forming a first electrode on a portion of a substrate assembly;

forming a high dielectric material over at least a portion of the first electrode; and

forming a second electrode over the high dielectric material, wherein at least one of the first and second electrodes comprises a layer of a platinum:ruthenium alloy.

7. The method of claim 6, wherein the layer of platinum:ruthenium alloy is a layer of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995.

8. The method of claim 7, wherein x is in the range of about 0.90 to about 0.98.

9. The method of claim 8, wherein x is about 0.95.

10. The method of claim 1, wherein forming the at least one of the first electrode and second electrode comprising the layer of platinum(x):ruthenium(1-x) alloy includes forming the layer of platinum(x):ruthenium(1-x) alloy by chemical vapor deposition.

11. A method for use in the formation of a capacitor, the method comprising:

providing a silicon containing surface of a substrate assembly;

forming a first electrode on a least a portion of the silicon containing surface of the substrate assembly, the first electrode including a layer of platinum(x):ruthenium(1-x) alloy;

providing a high dielectric material over at least a portion of the first electrode; and

providing a second electrode over the high dielectric material.

12. The method of claim 11, wherein the first electrode is a single layer of platinum (x) and ruthenium (1-x) alloy.

13. The method of claim 12, wherein a thickness of the layer is in a range of about 100Å to about 500Å.

14. The method of claim 11, wherein the step of forming the first electrode includes depositing the layer of platinum (x):ruthenium (1-x) alloy by chemical vapor deposition.

15. The method of claim 11, wherein x is in the range of about 0.60 to about 0.995.

16. The method of claim 15, wherein x is in the range of about 0.90 to about 0.98.

17. The method of claim 11, wherein the first electrode includes the layer of platinum(x):ruthenium(1-x) alloy and one or more additional conductive layers.

18. The method of claim 17, wherein the one or more additional conductive layers are formed from materials selected from the group of metals and metal alloys; metal and metal alloy oxides; metal nitrides; and metal silicides.

19. A method for use in forming a storage cell including a capacitor, the method comprising:

providing a substrate assembly including at least one active device; and

forming a capacitor relative to the at least one active device, the capacitor comprising at least one electrode including a barrier layer of platinum(x):ruthenium(1-x) alloy.

20. The method of claim 19, wherein forming the at least one electrode includes depositing the barrier layer of platinum (x):ruthenium(1-x) alloy by chemical vapor deposition.

21. The method of claim 19, wherein x is in the range of about 0.60 to about 0.995.

22. The method of claim 21, wherein x is in the range of about 0.90 to about 0.98.

23. A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a barrier layer over at least a portion of the surface, wherein the barrier layer is formed of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995.

24. The structure of claim 23, wherein x is in the range of about 0.90 to about 0.98.

25. The structure of claim 24, wherein x is about 0.95.

26. The structure of claim 23, wherein the portion of the surface is a silicon containing surface.

27. A capacitor structure comprising:

a first electrode;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a barrier layer of platinum(x):ruthenium(1-x) alloy.

28. The structure of claim 27, wherein x is in the range of about 0.60 to about 0.995.

29. The structure of claim 28, wherein x is in the range of about 0.90 to about 0.98.

30. The structure of claim 27, wherein at least one of the first electrode and second electrode comprises the barrier layer of platinum(x):ruthenium(1-x) alloy and one or more additional conductive layers.

31. The structure of claim 30, wherein the one or more additional conductive layers are formed from materials selected from materials selected from the group of metals and metal alloys; metal and metal alloy oxides; metal nitrides; and metal silicides.

32. A memory cell structure comprising:

a substrate assembly including at least one active device; and

a capacitor formed relative to the at least one active device, the capacitor comprising at least one electrode including a barrier layer formed of platinum(x):ruthenium(1-x) alloy.

33. The structure of claim 32, wherein the capacitor includes:

a first electrode formed relative to a silicon containing region of the at least one active device;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein the first electrode comprises the barrier layer formed of platinum(x):ruthenium(1-x) alloy.

34. The structure of claim 33, wherein the first electrode comprising the barrier layer formed of platinum(x):ruthenium(1-x) alloy includes one or more additional conductive layers.

35. The structure of claim 33, wherein x is in the range of about 0.60 to about 0.995.

36. The structure of claim 35, wherein x is in the range of about 0.90 to about 0.98.

37. A integrated circuit structure comprising:

a substrate assembly including at least one active device; and

an interconnect formed relative to the at least one active device, the interconnect including a barrier layer formed of platinum(x):ruthenium(1-x) alloy.

38. The structure of claim 37, wherein x is in the range of about 0.60 to about 0.995.

39. The structure of claim 38, wherein x is in the range of about 0.90 to about 0.98.